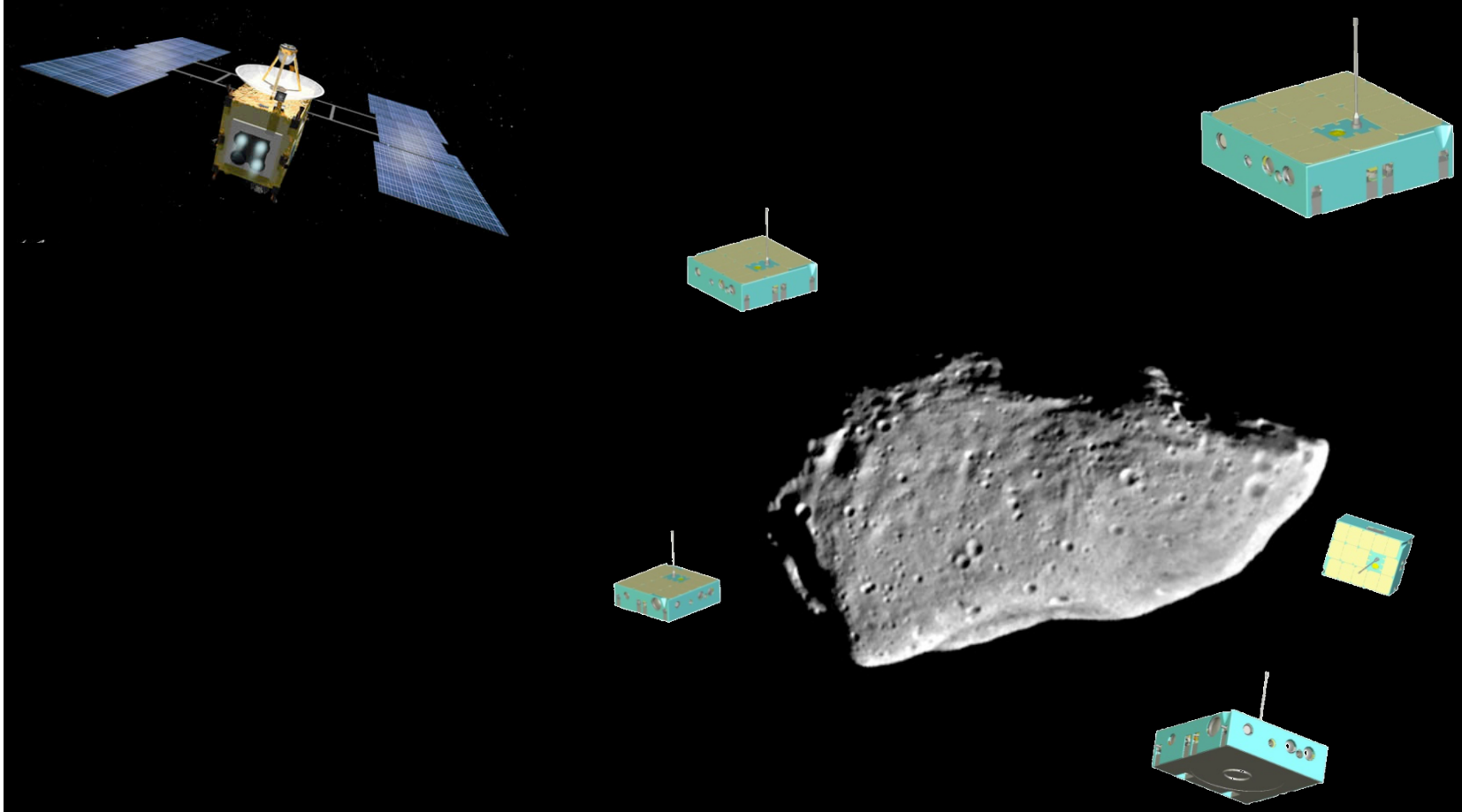
Miniaturizing Avionics Technologies for Small Body Missions



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Small Body Missions

- In Situ Characterization
- Remote Characterization
- Sample Return
- NEO Grand Tour/Rendezvous with Probes
- Typical Targets:
  - Asteroid Belt, Trojans
  - Main Belt Comets
  - Martian Moons
  - Irregular Satellites
  - Ice Dwarf Planets
  - Centaurs and Trans Neptune Objects
  - Interplanetary Dust
- Poorly Known and Unstable Environments
- Low Bandwidth Data Links
- Long Round Trip Communication Delays
- Cold, Natural Space Radiation Environment

Required Avionics Characteristics

- Low Power/Mass/Volume
  - Small to medium sized spacecraft
  - Minimize structure, cabling, support
  - Margin for Instruments and Propulsion
  - Accommodate in situ instruments, daughter craft, multi-platform missions
- Radiation Tolerant
  - Radiation tolerant (MRad not required)
  - Minimize power & cost, maximize performance
- Extreme Temperature (cold) Tolerant
  - Eliminate need for thermal management system (power/mass)
- Reusable From Mission To Mission
  - Reduce cost of avionics and support
- Adaptable and Reconfigurable
  - Minimize avionics
  - Support Fault Tolerance and Degraded Mode
- High Performance
  - Support multiple instruments
  - Support onboard instrument data processing
  - Support autonomous operations
- Fault Tolerant and Degraded Mode Capable
- Highly Efficiency, Low Mass, Power Generation

A radically new approach to spacecraft avionics will be required

Avionics Technologies for Small Body Missions

- Emerging Technologies for Cold Capable Avionics
  - Reduces or eliminates need for thermal management system (power and mass)
  - Provides additional degree of freedom in s/c configuration
  - Provides additional degree of freedom in mission operations
  - Reduces overall mission cost
  - Improves s/c robustness and reliability

  → Cold Blooded Spacecraft

- Advanced Electronics Technologies for Spacecraft Avionics
  - Enables custom low power ASICs at "reasonable" cost and schedule
  - Enables power, mass, volume reduction of s/c avionics
  - Enables flexible s/c architectures and operations

  → Avionics Subsystem On a Chip

- Emerging Computing Technologies
  - Enables onboard instrument data processing, science data processing, autonomous operations
  - Provides enhanced power management and low power operations
  - Provides enhanced reliability and system robustness
  - Provides flexible mission operations

  → Autonomous Spacecraft

  - Potentiates reduced system mass, power, volume

  → Ultra-Low-Power Computing

- Advanced Packaging Technologies
  - Reduces avionics mass and volume
  - Enables extreme temperature operation
  - Potentiates ultra low power avionics

  → Avionics System in Package

More Science. Smaller, Lower Power Spacecraft. Lower Cost Missions

0.5u SiGe Low Temperature Capable Mixed Signal ASICs for Space

The X-33 Remote Health Unit, circa 1998

SiGe

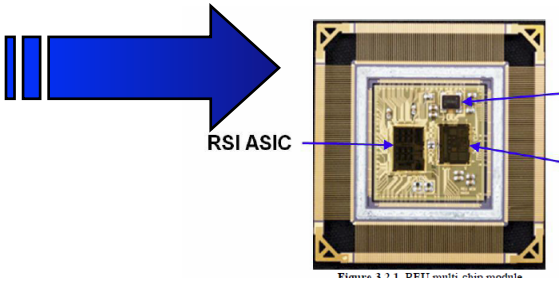
The ETDP Remote Electronics Unit, circa 2009

REU in connector housing!

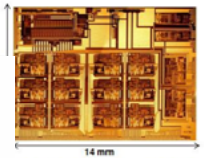
Analog front end die

Digital control die

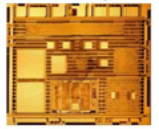
Conceptual integrated REU system-on-chip SiGe BiCMOS die



CRYO-5 SiGe Analog ASIC



CRYO-5 SiGe Digital ASIC



Specifications

- 5" x 3" x 6.75" = 101 in^3
- 11 kg
- 17 Watts
- -55°C to +125°C

Goals

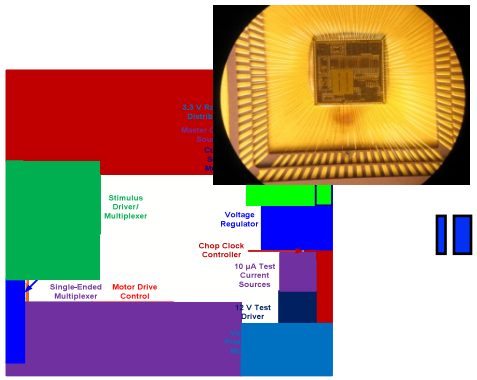
- 1.5" x 1.5" x 0.5" = 1.1 in^3 **(100x)**
- < 1 kg **(10x)**
- < 2 Watts **(10x)**
- **-180°C to +125°C, rad tolerant**

Supports Many Sensor Types:
Temperature, Strain, Pressure, Acceleration, Vibration, Heat Flux, Position, etc.

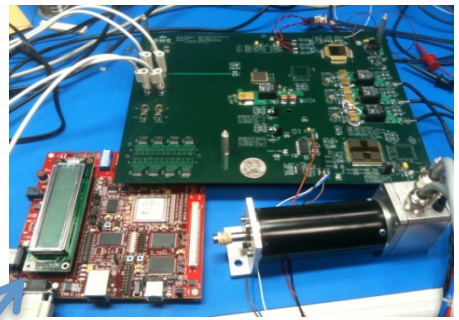
Use This REU as a Remote Vehicle Health Monitoring Node

10x Reduction in Size and Power
Elimination of Thermal Management System

Cold Capable Distributed Motor Controller: 0.5u SiGe + Quick Turn Rad Hard ASIC

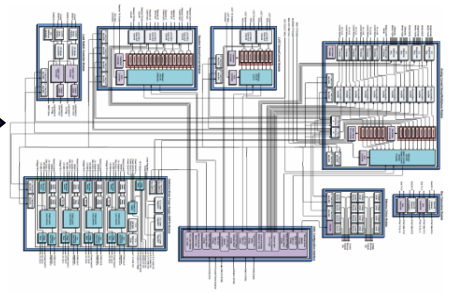


Analog Building Block Test Chip
Motor current sense
Voltage reference
Analog multiplexer
Operational amplifiers
Position sensor interfaces



Distributed System Test Bed
Scalable to >45 motors
Fault tolerant
Programmable

FPGA ->.35u SOICMOS ASIC

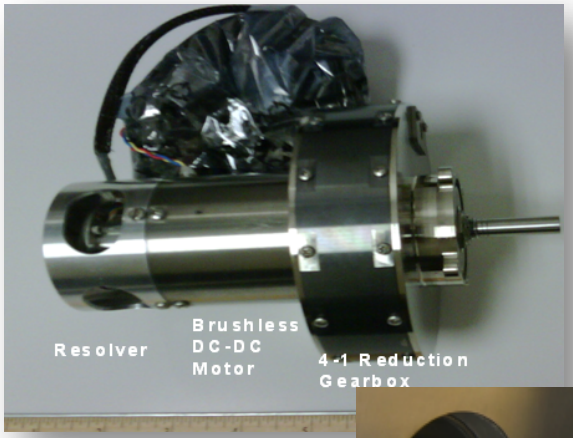


Brushless DC Motor Control ASIC
-180 to +120 C
< 2W total power dissipation
Motor size invariant
Tapes out Feb 2011

Distributed scalable modular architecture
High efficiency power distribution and conditioning
Low power, galvanic-isolated communication system
Reusable standard cell analog library
Cold cycle resistant packaging

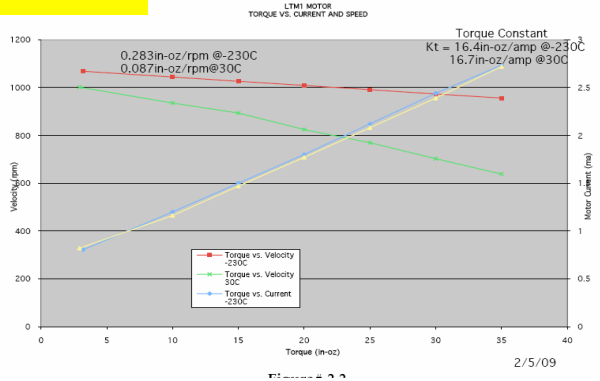
Next step – Develop 130nm SiGe Mixed Signal Library

Cold Capable Actuators

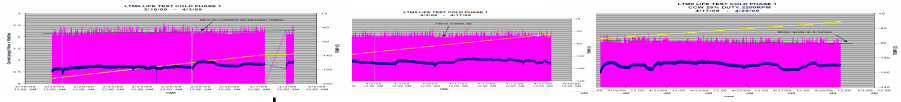


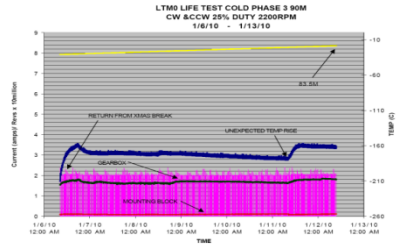
Motor-Resolver-Gearbox (4:1 Reduction)
Dry Lube Technology
Life Test at -200 C
JPL, LaRC, GRC, Aeroflex

Eliminates Heater Power and Mass



Motor Current and Torque Constant Over 100M Rev at -200C



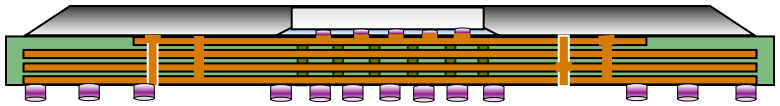


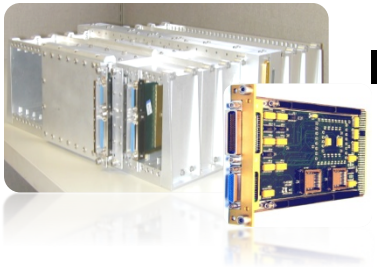
Mrevs 10M 20M 30M …….. 90M

Next Step – Mass/Weight Reduction using novel cold resistant alloys

Advanced Packaging Technologies

Flip Chip on LTCC





Through-silicon Via

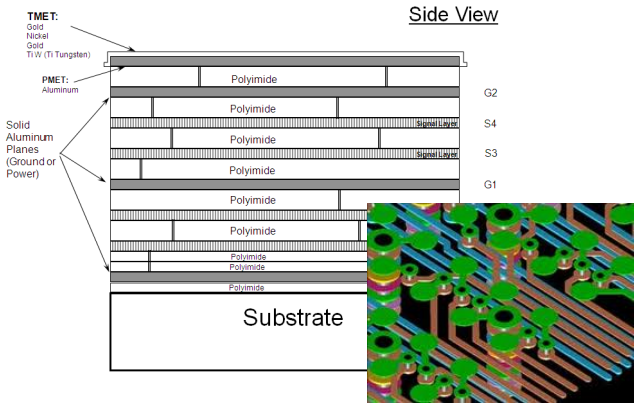
Stacked Multiple Mixed Technologies

80% Reduction In Avionics Mass and Volume

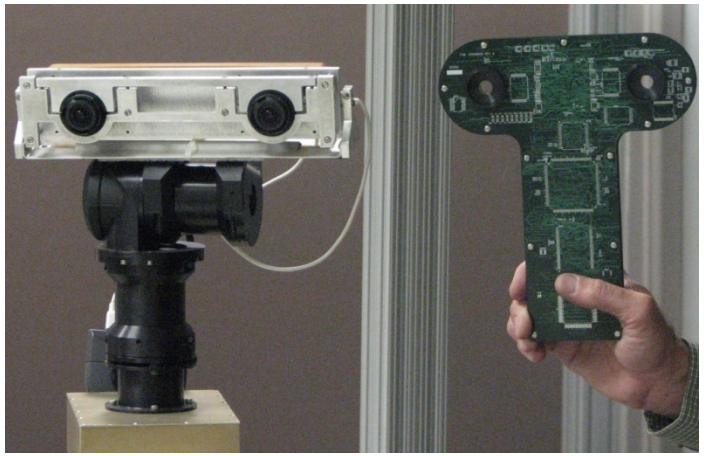
- Through-Silicon Via Stacked ICs
- High Density Interconnect
- Flip Chip Bonding
- Multi-function Structures
- Commercially Available

Space Qualification Required

High Density Interconnect(HDI)



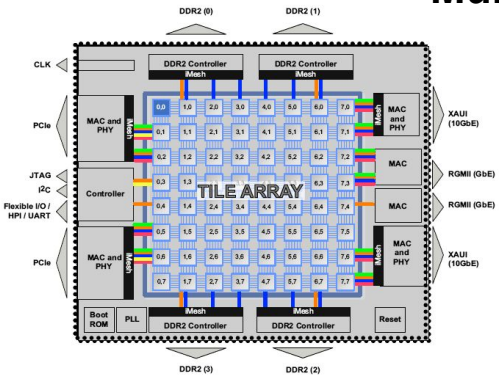
Multi-function Structures



Emerging Computing Technologies

Enabled by CMOS RHBD

Multicore Computing

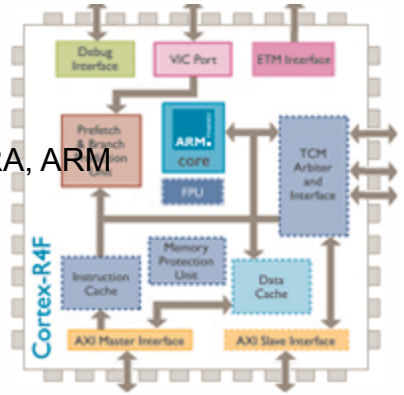


OPERA Maestro
49 Core
40 GOPS
“Cluster on a Chip”
>40Gb/s I/O
Linux & VxWorks
Power Scalable
Rad Hard
NRO, Boeing, ISI, Draper, Tilera

Needs 2nd Spin and Qualification

Low Power Computing

Cortex R4 Processor
>1M Drystones
<<1Watt
Rad Hard
Boeing, DARPA, DTRA, ARM



Needs Cold Characterization, Processor Design Completion and Qualification

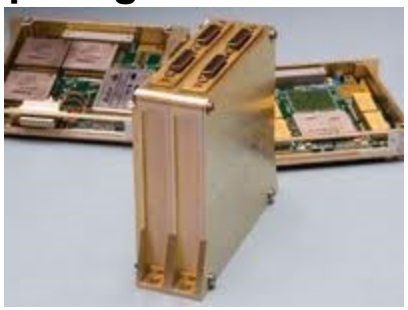
Next Step – Port to Next Gen RHBD Process
and
Add NASA/SBAG-Unique Design Improvements

Emerging Computing Technologies

Reconfigurable Computing

AFRL
Xilinx

Xilinx V5 QV 'SIRF' FPGA
RHBD 65 nm CMOS
130k Logic Cells
450MHz
3.12Gb Tx
Partial Reconfiguration



GSFC Space Cube
Xilinx V5 Stack
Reconfigurable computer

Advanced Spacecraft Interconnect

Multiple standards and products in development:

- Space Fiber (GSFC/ESA)
- Fiber Optic Ring Bus (AFRL, JPL, Space Photonics)
- Rapid I/O Based Interconnect (Seakr, BAE, JPL, LMCo, Honyewell)

Desired:

- 100Mb/s to 10Gb/s power scalable technology
- Light weight protocol (low power, low gate count)
- Hardware implementation (BIU)
- Multi-media (fiber optic, copper, wireless)

Standards organization being formed (AFRL, NASA, NRO…)

Next Steps – NASA Standard Reusable Plug n Play IP Libraries and NASA-led Advanced Avionics Interconnect Standard

Summary

Radio
Gyro
GPS
Camera
Computer
Data Recorder

- To miniaturize the vehicle, reduce the need for thermal management
  - Cold capable, miniaturized electronics
    - 0.5u SiGe today, 130nm SiGe in future
- To miniaturize electronics, use
  - Commercial process based RHBD ASICs
  - Advanced packaging
    - Stacked silicon using through-via technology
    - HDI interconnect
    - Flip-chip on LTCC
    - Multi-function structures
- To enable new types of missions and to dramatically increase science/$, use
  - Multicore power-scalable and ultra low power computing
  - Reconfigurable computing
  - Autonomy
- To minimize cost develop
  - Modular, reusable, plug and play building blocks
  - Standardized, low power, scalable interfaces and networks

State of the art electronics technologies can shrink avionics and spacecraft by orders of magnitude, while providing greatly increased capability and science/dollar